

Docket No.: 42390P7017

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
James P. Kardach	)	Examiner: Banankhah, Majid A.
	)	
Application No.: 09/606,839	)	Art Group: 2127
	)	
Filed: June 28, 2000	)	
	)	
For: Method and Apparatus for Providing	)	
Real-Time Operation in a Personal	)	
<u>Computer System</u>	)	

APPEAL BRIEF  
IN SUPPORT OF APPELLANT'S APPEAL  
TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicant (hereinafter "Appellant") hereby submits this Brief in support of its appeal from a final decision by the Examiner, mailed November 18, 2004, in the above-referenced Application. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interferences for allowance of the above-captioned patent application.

An oral hearing is not desired.

04/21/2005 EFLORES 00000021 09606839

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**I. REAL PARTY IN INTEREST**

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

**II. RELATED APPEALS AND INTERFERENCES**

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

**III. STATUS OF THE CLAIMS**

Claims 1-20 are currently pending in the above-referenced application. In the Final Office Action mailed November 18, 2004, claims 1-11, 13-15, and 19-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over MacDonald (U.S. Patent No. 6,295,574) ("*MacDonald*") in view of Simpson (EP. Pat No. 0742522A) ("*Simpson*"). In addition, claims 12 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *MacDonald* in view of *Simpson*, further in view of Williams et al. (U.S. Patent No. 5,764,582) ("*Williams*"). Claims 1-20 are being appealed.

**IV. STATUS OF AMENDMENTS**

Claims 1-20 are currently pending in the subject application. These claims were finally rejected in the Final Office Action mailed November 18, 2004

Appellant respectfully traverses each of these grounds of rejection.

**V. SUMMARY OF THE CLAIMED SUBJECT MATTER**

According to one embodiment, a method is described. The method includes receiving real-time analog data at a personal computer implementing a general purpose operating system. Subsequently, a real-time interrupt indicating a request is generated to process the real-time data at a central processing unit (CPU). It is then determined whether the real-time interrupt has a higher priority than a non-real time operation already being processed at the CPU. If the real-time data has a higher priority, the CPU then processes the real-time data. See page 8, lines 19-23 – page 9, lines 1-11.

In a further embodiment, a computer system is described. The computer system includes a chipset, a bus, and a CPU. The chipset and CPU are coupled to the bus. The CPU generates a real-time interrupt upon receiving real-time analog data. If the real-time interrupt has a higher priority than a non-real-time operation currently being processed, the real-time data is processed. Id.

**VI. GROUND OF REJECTION TO BE REVIEWED ON APPEAL**

Claims 1-11, 13-15, and 19-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *MacDonald* in view of *Simpson*.

Claims 12 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *MacDonald* in view of *Simpson*, further in view of *Williams*.

## VII. ARGUMENT

1. **THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE ANY COMBINATION OF *MACDONALD* AND *SIMPSON* DOES NOT DISCLOSE OR SUGGEST DETERMINING WHETHER THE REAL-TIME INTERRUPT HAS A HIGHER PRIORITY THAN A NON-REAL TIME OPERATION BEING PROCESSED AT A CPU**

Appellant respectfully submits that *MacDonald* in view of *Simpson* fails to disclose or suggest the claimed invention for the reasons set forth below. As the Honorable Board is well aware, in order to establish a *prima facie* case of obviousness:

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.” (Emphasis added). *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8<sup>th</sup> Edition, Revision 2, May 2004, §2143.

- (A) **Claims 1-11, 13-15, and 19-20 were improperly rejected because *MacDonald* in view of *Simpson* does not disclose determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU**

Claims 1-11, 13-15, and 19-20 are not obvious in view of *MacDonald* and *Simpson* under 35 U.S.C. §103(a). For example, Appellant’s claim 1 recites the following:

A method comprising:

- receiving real-time analog data at a personal computer implementing a general purpose operating system;

- generating a real-time interrupt indicating a request to process the real time data at a central processing unit (CPU);

- determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU; and

- processing the real-time data if the real-time interrupt has a higher priority than the non-real time operation.

Appellant's claim 7 recites:

A computer system comprising:

- a chipset;

- a bus coupled to the chipset; and

- a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

Appellant's claim 13 recites:

A central processing unit (CPU) comprising:

- a timer to generate timing signals at predetermined time intervals;

- a register to store real-time data received at the CPU as analog data;

- an event mechanism coupled to the timer and the register to generate real-time interrupts in response to receiving the timing signals and determining that real-time data is stored within the register; and

- an event handler coupled to the event mechanism to process data associated with the real-time interrupts received from the event mechanism upon determining the relative priority between the real-time interrupts and non-real-time operations being processed.

*MacDonald* discloses a CPU that includes a real time interrupt (RTI) control unit configured to control real time interrupt capabilities of the CPU. Upon receipt of a real



time interrupt signal via an RTI pin, the RTI control unit interrupts the currently executing instructions at an instruction boundary in order to execute the interrupt service routine. See *MacDonald* at Abstract ll. 1-6.

However, *MacDonald* does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. In fact, the Examiner, in the Final Office Action admits that *MacDonald* fails to explicitly teach of a step or means for determining the real time interrupt has a higher priority than a non-real time operation being processed at the CPU. See Final Office Action, mailed November 18, 2004, at page 3, paragraph 1. Instead, the Examiner cites *Simpson* as including such a feature.

*Simpson* discloses control circuitry for, and a method of controlling, multiple priority level interrupt requests to a microprocessor in which output circuitry for outputting an interrupt identifier is operable only in response to an interrupt signal having a higher priority status than any currently executing interrupt process. See *Simpson* at Abstract. *Simpson* further discloses arbiter circuitry connected to storage circuitry for determining the priority status for each interrupt signal. See *Simpson* at col. 1, ll. 46-48. Nonetheless, *Simpson* does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

Even though *Simpson* discloses a processor interrupt control system that determines the priority of interrupts, the interrupts are not real-time interrupts. Real-time interrupts are very time sensitive and therefore require much faster processing than do non real-time interrupts. A system designed to handle non real-time interrupts, as disclosed in *Simpson*, could not be used to handle the addition of real-time interrupts.

The Examiner asserts that

It would have been obvious for one ordinary in the art at the time the invention was made to use priority determination scheme of *Simpson* in real time interrupt handling system of *MacDonald*.

See Final Office Action, mailed November 18, 2004 at page 4, paragraph 1. Appellant respectfully disagrees with the Examiner's combining of *MacDonald* and *Simpson*. As discussed above, the system of *Simpson* would not be able to be combined with the system of *MacDonald* to handle real-time interrupts.

Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 1-11, 13-15, and 19-20 under 35 U.S.C. §103(a) as being obvious over the combination of *MacDonald* and *Simpson* should be reversed.

Claims 2-6 and 17-18 depend from claim 1, claims 8-12 and 19-20 depend from claim 7, and claims 14-16 depend from claim 13. Given that dependent claims necessarily include the limitations of the claims from which they depend, Appellant submits that the invention as claimed in claims 2-6, 8-12, 14-16, and 17-20 are similarly patentable over *MacDonald* in view of *Simpson*.

Thus, the Examiner erred in rejecting claims 1-11, 13-15, and 19-20 under 35 U.S.C. § 103(a).

**2. THE PENDING CLAIMS WERE IMPROPERLY REJECTED UNDER 35 U.S.C. § 103(a) BECAUSE ANY COMBINATION OF *MACDONALD*, *SIMPSON* AND *WILLIAMS* DOES NOT DISCLOSE OR SUGGEST DETERMINING WHETHER THE REAL-TIME INTERRUPT HAS A HIGHER PRIORITY THAN A NON-REAL TIME OPERATION BEING PROCESSED AT A CPU**

Appellant respectfully submits that *MacDonald* in view of *Simpson* in further view of *Williams* fails to disclose or suggest the claimed invention for the reasons set forth below.

**(A) Claims 12 and 16-18 were improperly rejected because *MacDonald* in view of *Simpson* in further view of *Williams* does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU**

Claims 12 and 16-18 are not obvious in view of *MacDonald*, *Simpson* and *Williams* under 35 U.S.C. §103(a).

As discussed above, nowhere does *MacDonald* or *Simpson* teach or suggest each and every element of the Appellants' independent claims. For example, *MacDonald* and *Simpson* do not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU.

*Williams* discloses a bus that is provided to communicate data between a digital signal processor and a hardware interface, which includes digital-to-analog and analog-to-digital converters. Inputs and outputs for the various multimedia end devices are connected through the digital-to-analog and analog-to-digital converter. See *Williams* at Abstract.

Nevertheless, *Williams* does not disclose or suggest determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. Since *MacDonald* and *Simpson* fail to disclose all of the elements included in the

Appellant's independent claim, including claim 1, and since *Williams* fails to disclose or suggest those elements missing from *MacDonald* and *Simpson*, the combination of *MacDonald*, *Simpson*, and *Williams* fails to disclose or suggest each and every element of the Appellant's invention as embodied in the claims. Consequently, the Examiner has not established a prima facie case of obviousness, and the Examiner's rejection of claims 12 and 16-18 under 35 U.S.C. §103(a) as being obvious over the combination of *MacDonald*, *Simpson*, and *Williams* should be reversed.

### **VIII. CONCLUSION**


Careful review of the Examiner's rejections shows that the Examiner has failed to provide any reference, or combination of references of the prior art that shows all of the elements of each appealed claim. Therefore, Appellants respectfully submit that all appealed claims in this application are patentable and were improperly rejected by the Examiner during prosecution before the United States Patent and Trademark Office. Appellants respectfully request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

This brief is submitted with a check for \$500.00 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

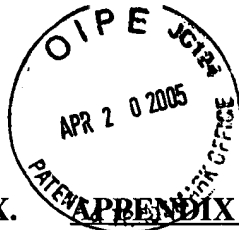
Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: \_\_\_\_\_

  
\_\_\_\_\_  
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IX. APPENDIX OF CLAIMS (37 C.F.R. § 41.37(c)(1)(viii))

The claims on appeal read as follows:

1. A method comprising:

receiving real-time analog data at a personal computer implementing a general purpose operating system;

generating a real-time interrupt indicating a request to process the real time data at a central processing unit (CPU);

determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU; and

processing the real-time data if the real-time interrupt has a higher priority than the non-real time operation.

2. The method of claim 1 further comprising continuing to process the non-real time operation if the real-time interrupt does not have a higher priority than the non-real time operation.

3. The method of claim 1 further comprising:

saving the state of the non-real time operation at the personal computer prior to processing the data associated with the real-time interrupt; and

processing the non-real time operation after processing of the data associated with the real-time interrupt has been completed.

4. The method of claim 1 further comprising:

receiving a non-real time interrupt while processing the real-time interrupt; and

determining whether the non-real time interrupt has a higher priority than the real-time interrupt.

5. The method of claim 4 further comprising:

continuing the processing of the real-time interrupt if the non-real time interrupt does not have a higher priority than the real time interrupt.

6. The method of claim 4 further comprising:

terminating the processing of the real-time interrupt if the non-real time interrupt has a higher priority; and

processing the non-real time interrupt.

7. A computer system comprising:

a chipset;

a bus coupled to the chipset; and

a central processing unit (CPU), coupled to the bus, to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed.

8. The computer system of claim 7 wherein the CPU comprises:

a timer to generate timing signals at predetermined time intervals; and

an event mechanism coupled to the timer to generate the real time interrupts.

9. The computer system of claim 8 wherein the CPU further comprises an event handler coupled to the event mechanism to process the real-time interrupts.

10. The computer system of claim 9 wherein the CPU further comprises a register coupled to the event mechanism to store real-time data.

11. The computer system of claim 9 wherein the event mechanism determines the relative priority between the real-time interrupts and the non-real-time operations.

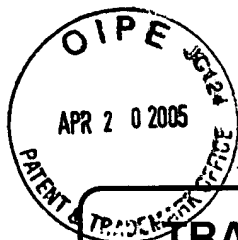
12. The computer system of claim 11 wherein the CPU further comprises an analog to digital converter coupled to the register.

13. A central processing unit (CPU) comprising:
- a timer to generate timing signals at predetermined time intervals;
  - a register to store real-time data received at the CPU as analog data;
  - an event mechanism coupled to the timer and the register to generate real-time interrupts in response to receiving the timing signals and determining that real-time data is stored within the register; and
- an event handler coupled to the event mechanism to process data associated with the real-time interrupts received from the event mechanism upon determining the relative priority between the real-time interrupts and non-real-time operations being processed.
14. The CPU of claim 13 wherein the real-time analog data is data received from an analog radio coupled to the CPU.
15. The CPU of claim 13 wherein the event handler verifies whether there is data stored in register upon detecting a real-time interrupt and determines the priority of the real-time interrupt relative to other interrupts received.
16. The CPU of claim 13 wherein the CPU further comprises an analog to digital converter coupled to the register to convert the real-time analog data to digital data.
17. The method of claim 1 wherein receiving the real-time analog data comprises:
- converting the real-time analog data to digital data; and
  - storing the digital data at a register.
18. The method of claim 17 wherein generating the real-time interrupt comprises:
- receiving a timing signal at an event mechanism at a predetermined interval;
  - the event mechanism determining whether data is stored within the register; and
  - generating the real-time interrupt if data is stored within the register



19. The computer system of claim 10 wherein the event mechanism generates the real time interrupts in response to receiving the timing signals from the timer and determining that real-time data is stored within the register.

20. The computer system of claim 7 wherein the real-time analog data is data received from an analog radio.



AF 2127

<b>TRANSMITTAL FORM</b> <i>(to be used for all correspondence after initial filing)</i>		Application No.	09/606,839
		Filing Date	June 28, 2000
		First Named Inventor	James P. Kardach
		Art Unit	2127
		Examiner Name	Banankhah, Majid A
Total Number of Pages in This Submission	20	Attorney Docket Number	42390P7017

ENCLOSURES (check all that apply)		
<input checked="" type="checkbox"/> Fee Transmittal Form <input checked="" type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment / Response <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement <input type="checkbox"/> PTO/SB/08 <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Response to Missing Parts/Incomplete Application <input type="checkbox"/> Basic Filing Fee <input type="checkbox"/> Declaration/POA <input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s)	<input type="checkbox"/> After Allowance Communication to Group <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input checked="" type="checkbox"/> Other Enclosure(s) (please identify below): <div style="border: 1px solid black; padding: 5px; margin-top: 5px;">-First Class Certificate of Mailing; and -Stamped return postcard.</div>
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT	
Firm or Individual name	Mark L. Watson, Reg. No. 46,322 <b>BLAKELY, SOLOKOFF, TAYLOR &amp; ZAFMAN LLP</b>
Signature	
Date	April 18, 2005

CERTIFICATE OF MAILING/TRANSMISSION	
I hereby certify that this correspondence is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.	
Typed or printed name	Krista Mathieson
Signature	
Date	April 18, 2005



# FEE TRANSMITTAL for FY 2005

Patent fees are subject to annual revision.

## Complete if Known

Application Number	09/606,839
Filing Date	June 28, 2000
First Named Inventor	James P. Kardach
Examiner Name	Banankhah, Majid A
Art Unit	2127
Attorney Docket No.	42390P7017

☐ Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$) 500.00

## METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit card ☐ Money Order ☐ None ☐ Other (please identify): \_\_\_\_\_

☒ Deposit Account Deposit Account Number: 02-2666 Deposit Account Name: Blakely, Sokoloff, Taylor & Zafman LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, except for the filing fee  
☒ Charge any additional fee(s) or underpayment of fee(s) ☒ Credit any overpayments  
under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

## FEE CALCULATION

### 1. EXTRA CLAIM FEES

	Extra Claims	Fee from below	Fee Paid
Total Claims	16	20*	0
Independent Claims	3	3*	0
Multiple Dependent			

Large Entity	Small Entity	Fee Code	Fee (\$)	Fee Description
1202	2202	50	25	Claims in excess of 20
1201	2201	200	100	Independent claims in excess of 3
1203	2203	360	180	Multiple Dependent claim, if not paid
1204	2204	300	150	**Reissue independent claims over original patent
1205	2205	300	150	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (1) (\$) 0.00

\*or number previously paid, if greater, For Reissues, see below

### 2. ADDITIONAL FEES

Large Entity	Small Entity	Fee Code	Fee (\$)	Fee Description
1051	2051	130	65	Surcharge - late filing fee or oath
1052	2052	50	25	Surcharge - late provisional filing fee or cover sheet.
2053	2053	130	130	Non-English specification
1251	2251	120	60	Extension for reply within first month
1252	2252	450	225	Extension for reply within second month
1253	2253	1,020	510	Extension for reply within third month
1254	2254	1,590	795	Extension for reply within fourth month
1255	2255	2,160	1,080	Extension for reply within fifth month
1401	2401	500	250	Notice of Appeal
1402	2402	500	250	Filing a brief in support of an appeal
1403	2403	1,000	500	Request for oral hearing
1451	2451	1,510	1,510	Petition to institute a public use proceeding
1460	2460	130	130	Petitions to the Commissioner
1807	1807	50	50	Processing fee under 37 CFR 1.17(q)
1806	1806	180	180	Submission of Information Disclosure Stmt
1809	1809	790	395	Filing a submission after final rejection (37 CFR § 1.129(a))
1810	2810	790	395	For each additional invention to be examined (37 CFR § 1.129(b))

Other fee (specify) \_\_\_\_\_

SUBTOTAL (2)

(\$) 500.00

## SUBMITTED BY

## Complete (if applicable)

Name (Print/Type)	Mark L. Watson	Registration No. (Attorney/Agent)	46,322	Telephone	(303) 740-1980
Signature		Date			04/18/05